2P0500

V1.02

2025 09

2P0500

1

2P0500 / SOC

A4

2P0500

2P0500

LA364 64 L1 Cache(I/D) 32KB L2 Cache 512KB 750MHz

LA132 32 400MHz

1 32 DDR3

2 10M/100M/1000M GMAC RGMII/MII

3 USB2.0 HOST 1 OTG

4 SPI 1

1 8 LSU

1 1 AFE/CIS

1 4 8 DA

4 I2C

8 UART

2 SDIO

40 PWM

3 PMIO

139 GPIO

1

RTC/HPET

DFS/DPM

1.2.2

32 DDR3 400MHz

32/16

1.2.3 USB

3 USB2.0 HOST

1 OTG

USB1.1 USB2.0

EHCI 480Mbps

OHCI

1.2.4 GMAC

10/100/1000Mbps MAC

IEEE 802.3

PHY RGMII/MII

/

Timestamp

CSMA/CD

CRC

1.2.5 SPI

4

(SPI0)

I/O SPI Flash

1.2.6 **UART**

1 UART TXD,RXD,CTS, RTS, DSR,DTR,DCD, RI

Ÿÿ3 8Ã UART

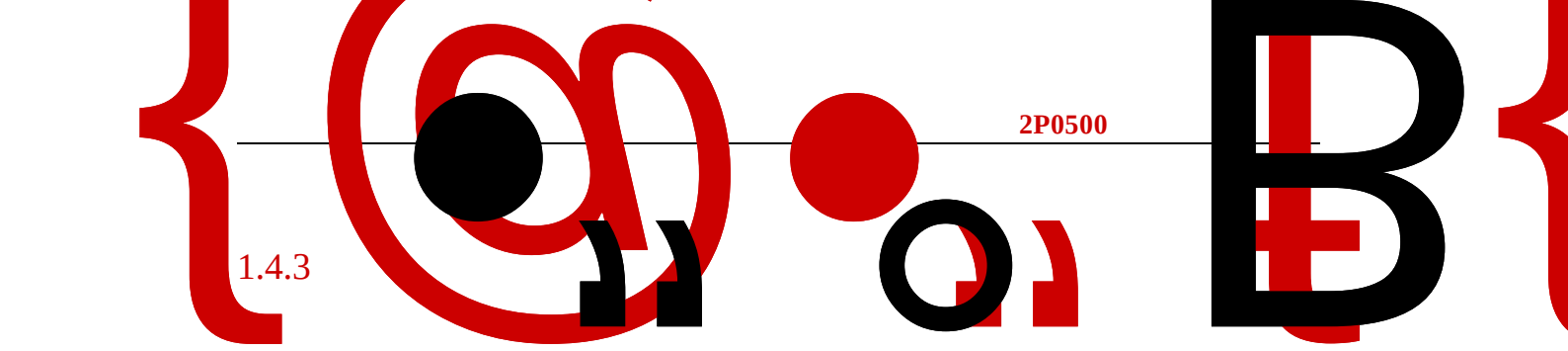
1.2.11 PMIO

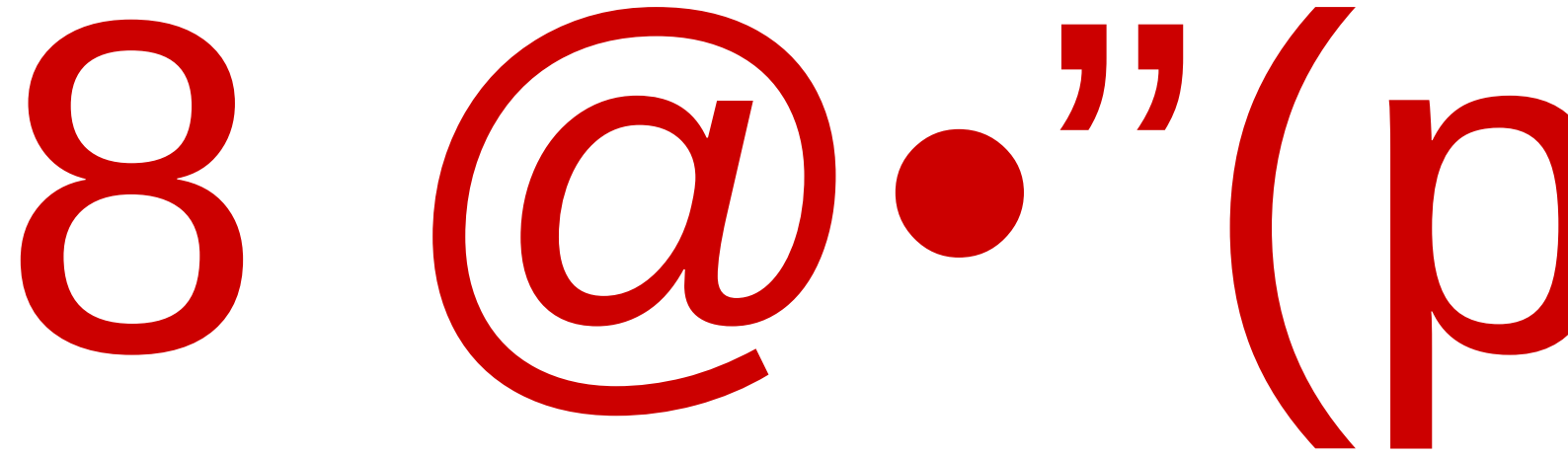
3 PMIO

80

† F אp

1.4.3





PRT_SPI_CSN	O	ôhx		VDD_3V3		
PRT_SPI_MOSI	O	ôhx		VDD_3V3		
PRT_SPI_MISO	I			VDD_3V3		
SCA_SPI_CLK	O	ôh0		VDD_3V3		
SCA_SPI_CSN	O	ôhx		VDD_3V3		
SCA_SPI_MOSI	O	ôhx		VDD_3V3		
SCA_SPI_MISO	I			VDD_3V3		

2.5 UART

UART[1:0]_TXD	O	ôh1		VDD_3V3		
UART[1:0]_RXD	I			VDD_3V3		
PRT_UART_TXD	O	ôh1		VDD_3V3		
PRT_UART_RXD	I			VDD_3V3		
SCA_UART_TXD	O	ôh1		VDD_3V3		
SCA_UART_RXD	I			VDD_3V3		

2P0500 (UART0)

(UART1) UART0 2x4 4x2

UART

UART1 1x4 2x2

2.16

2- 2

prt_uart0_rx	pm0io[0]	prt_pwm[0]	PRT_GPIO00
prt_uart0_tx	pm0io[1]	prt_pwm[1]	PRT_GPIO01
prt_i2c0_scl	pm0io[2]	prt_pwm[2]	PRT_GPIO02
prt_i2c0_sda	pm0io[3]	prt_pwm[3]	PRT_GPIO03
prt_i2c1_scl	prt_uart1_rx	prt_pwm[4]	PRT_GPIO04
prt_i2c1_sda	prt_uart1_tx	prt_pwm[5]	PRT_GPIO05
prt_spi_clk	gmac0_col	prt_pwm[6]	PRT_GPIO06
prt_spi_miso	gmac0_crs	prt_pwm[7]	PRT_GPIO07
prt_spi_mosi	gmac0_ptp_trig	prt_pwm[8]	PRT_GPIO08
prt_spi_cs	gmac0_ptp_pps	prt_pwm[9]	

sca_cisclk[2]	pm0io[28]	pm1io[28]	SCA_GPIO34
sca_cispls[0]	pm0io[29]	pm1io[29]	SCA_GPIO35
sca_cispwm	pm0io[30]	pm1io[30]	SCA_GPIO36

3.2 USB

2P0500 USB

USB Rev 1.1 USB Rev 2.0

OHCI Rev 1.0 EHCI Rev 1.0

LS Low Speed FS Full Speed HS High Speed USB

USB2.0

USB2.0 EHCI

OHCI EHCI

OHCI

EHCI

3.3 OTG

2P0500 OTG :

HNP SRP

DMA OTG

device 480Mbps

host 480Mbps

device 10 endpoint endpoint0

device 4 IN

host 12 channel channel

host periodic OUT

3.4 GMAC

2P0500 GMAC GMAC0 GMAC1

3.5 SPI

SPI

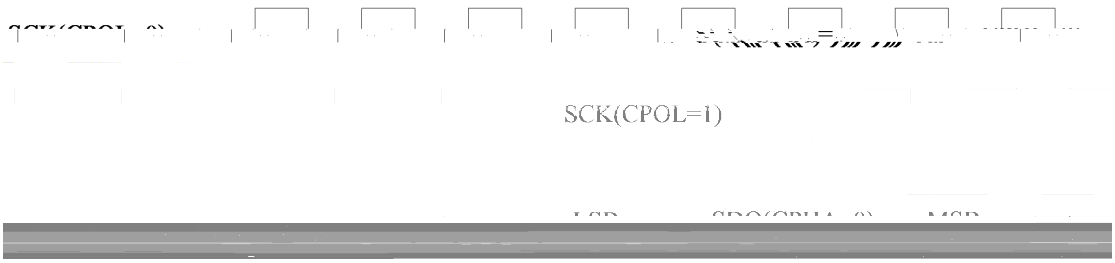
2P0500 SPI

SPI IO SPI Flash

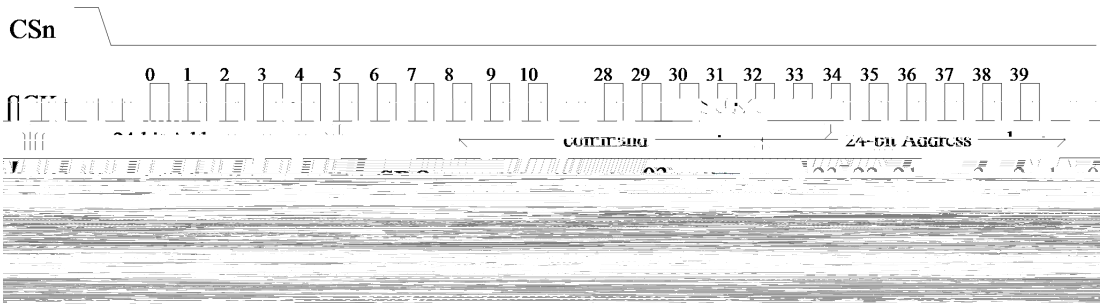
memory memory BOOT

SPI Flash

SPI



3.1 SPI



3.2 SPI Flash

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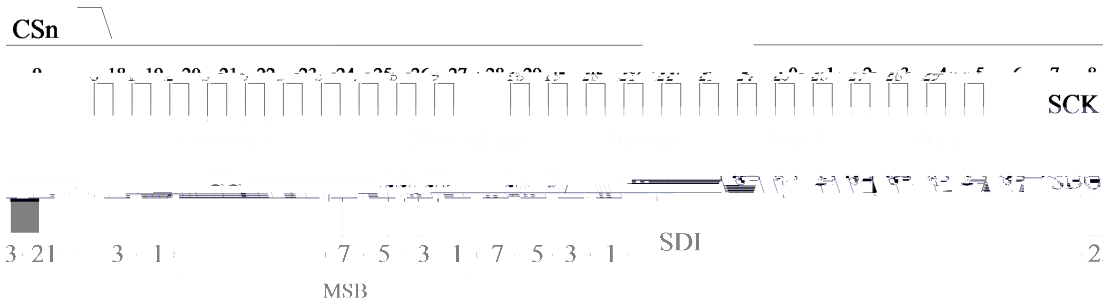
3.3 SPI Flash



3.4 SPI Flash I/O

3.6 UART

2P0500 8 UART 1 (UART0) 1

2 (UART2UAR T ¡)

3.7 I²C

2P0500 I2C

I2C SDA SCL

400kbps

3.8 PRINTER

2P0500 JBIG85 8

3.9 SCANNER

2P0500 RGB segment

CIS AFE

3.10 DA

2P0500 DA 4 8 DA

3.11 SDIO

2P0500 SDIO/eMMC SD/eMMC Memory SDIO

SDIO0 SD/eMMC Memory

SDIO

(512K Byte

)

3.12 PMIO

2P0500 IO Programmable Multifunction IO PMIO PMIO

PMIO PMIO Timer PWM Generator GPIO

3.13 PWM

2P0500 40 / PWM PWM PWM 32

3.14 GPIO

2P0500 139 GPIO

GPIO

3.15 HPET

2P0500 32 1 2

3.16 RTC

RTC

RTC 10

RTC 32.768KHZ

0.1

3.17

2P0500

(OTG)

Dynamic Power Management DPM

NODE CORE+SCACHE DDR IMAGE SCAN SYS

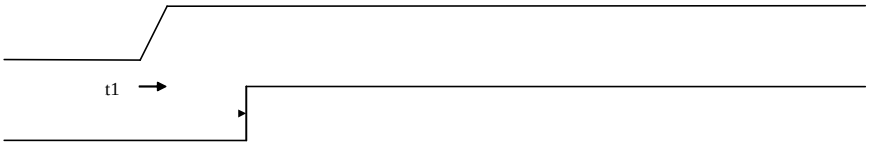
Dynamic Frequency Scaling DFS DFS

LA132

3

4

4.1



VDD_1V1_USB	USB vp	vptx	-0.

5.3 DDR3

5.3.1

5- 4

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	1.42	1.5	1.58	V
VDDQ	Supply Voltage for Output	1.42	1.5	1.58	V

5.3.2

5.3.2.1

5- 5

Symbol	Parameter	DDR3-800/1066/1333/1600		Unit
		Min	Max	
VIH.ac	3 ž			

5.3 ac-swing ac-level tDVA

5- 7

Symbol	Parameter	DDR3-800,1066		Unit
		Min	Max	
V_{IHdiff}	Differential input high	+ 0.200	note 3	V
V_{ILdiff}	Differential input logic low	Note 3	- 0.200	V
$V_{IHdiff(ac)}$	Differential input high ac	2 x (VIH(ac) - Vref)	Note 3	V
$V_{ILdiff(ac)}$	Differential input low ac	note 3	2 x (VIL(ac) - Vref)	V

5.3.2.3

CK CK DQS DQS 5- 8

VIX

VDD VSS

VOL AC VOH AC 5-11 5.4

5-11

Description	Measured from	Measured to	Defined by
Single-ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC) -VOL(AC)] / -H

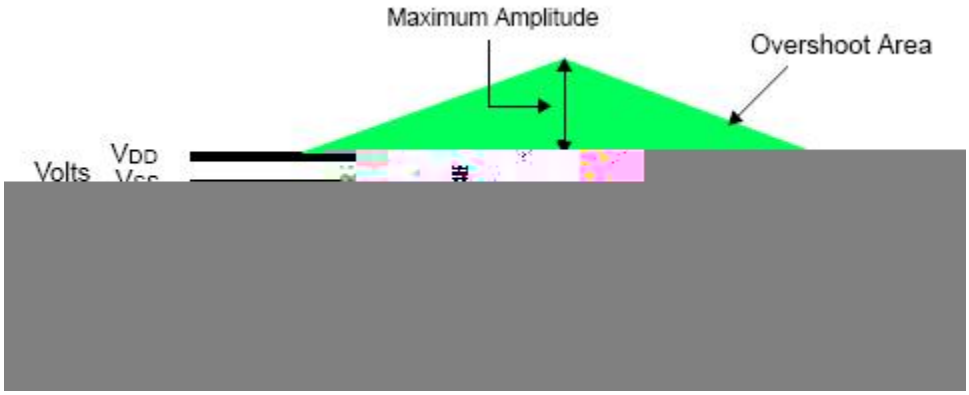
IJ

5.6

5- 14

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Differential Output Slew Rate	SRQdiff	5	10	5	10	5	10	TBD	10	V/ns

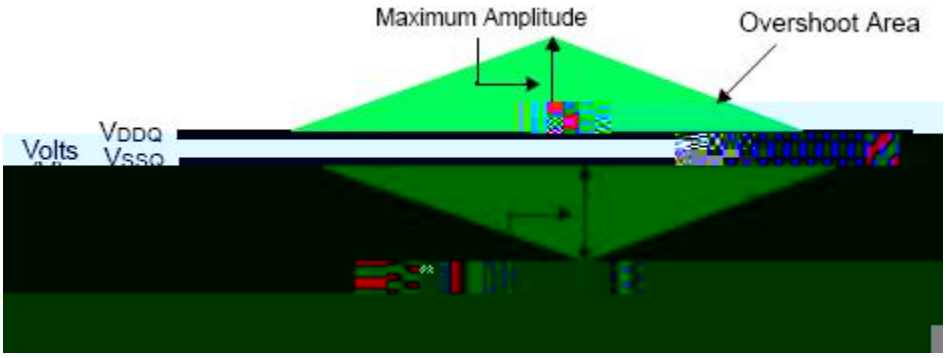
5.3.3.5



5.7

5- 16 /

	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units
Maximum peak amplitude allowed for overshoot area.	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area.	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDDQ	0.25	0.19	0.15	0.13	V-ns
Maximum undershoot area below VSSQ	0.25	0.19	0.15	0.13	V-ns
(CK, CK#, DQ, DQS, DQS#, DM)					



5.8

5.3.3.6 ODT

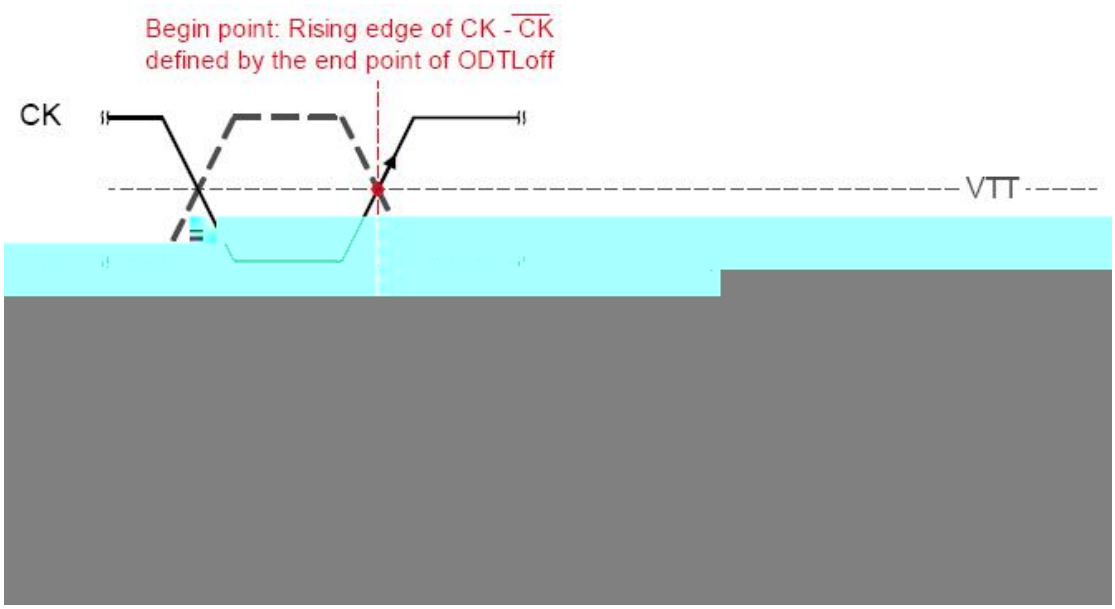
5- 17 ODT

Symbol	Begin Point Definition	End Point Definition	Figure
tAON	Rising edge of CK -CK# defined by the end point of ODTLon	Extrapolated point at VSSQ	Figure 103
tAONPD	Rising edge of CK -CK# with ODT being first registered high	Extrapolated point at VSSQ	Figure 104
tAOF	Rising edge of CK -CK#defined by the end point of ODTLoff	End point: Extrapolated point at VRTT_Nom	Figure 105
tAOFPD	Rising edge of CK -CK# with ODT being first registered low	End point: Extrapolated point at VRTT_Nom	Figure 106
tADC	Rising edge of CK -CK# defined by the end point of ODTLcnw, ODTLcwn4 or ODTLcwn8	End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively	Figure 107

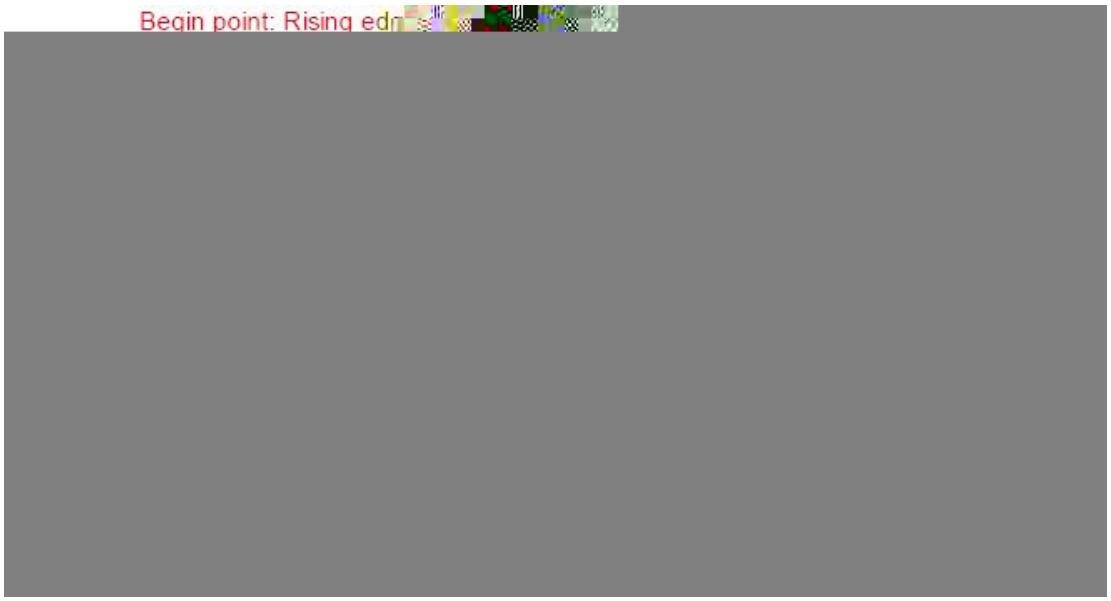
5- 18 ODT

Measured Parameter	RTT_Nom Setting	RTT_Wr Setting	VSW1[V]	VSW2[V]
tAON	RZQ/4	NA	0.05	0.10
	RZQ/12	NA	0.10	0.20
tAONPD	RZQ/4	NA	0.05	0.10
	RZQ/12	NA	0.10	0.20
tAOF	RZQ/4	NA	0.05	0.10
	RZQ/12	NA	0.10	0.20
tAOFPD	RZQ/4	NA	0.05	0.10
	RZQ/12	NA	0.10	0.20
tAD	RZQ/12	RZQ/2	0.20	0.30

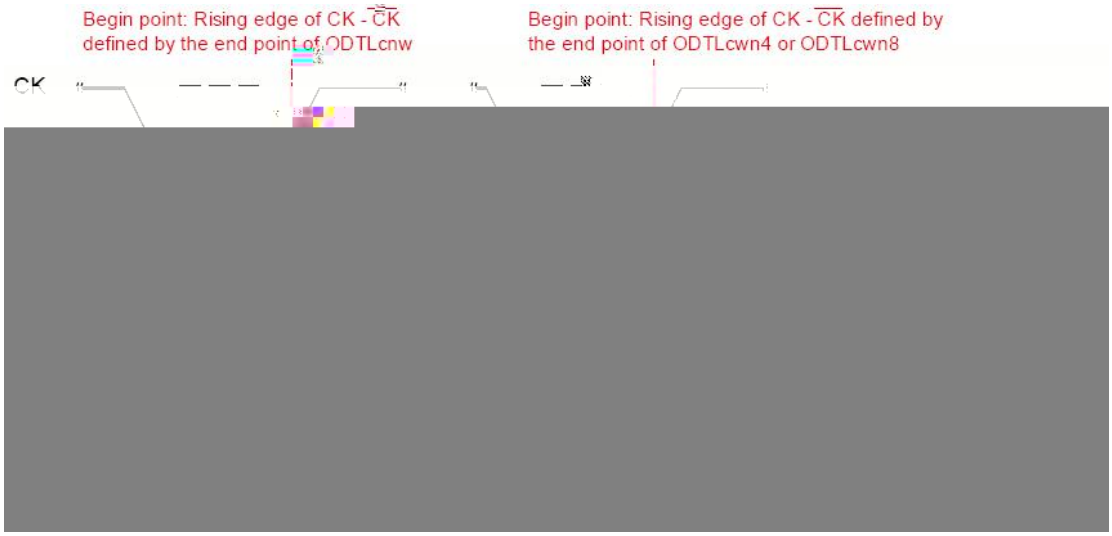
5.10 tAONPD



5.11 tAOF



5.12 tAOFPD



5.13 tADC

5.3.4 IDD IDDQ

5- 19 IDD IDDQ

Symbol	DDR3-800		DDR3-1066			DDR3-1333				DDR3-1600				Unit
	5-5-5	6-6-6	6-6-6	7-7-7	8-8-8	7-7-7	8-8-8	9-9-9	10-10-10	8-8-8	9-9-9	10-10-10	11-11-11	
tCK	2.5		1.875			1.5				1.25				ns
CL	5	6	6	7	8	7	8	9	10	8	9	10	11	nCK
nRCD	5	6	6	7	8	7	8	9	10	8	9	10	11	nCK
nRC	20	21	26	27	28	31	32	33	34	36	37	38	39	nCK
nRAS	15		20			24				28				n= î

5.3.5 /

5- 20 /

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Input/output capacitance (DQ, DM, DQS, DQS#, TDQS,TDQS#)	CIO	1.5	3.0	1.5	2.7	1.5	2.5	1.5	2.- غ	

55 l 5 ⊢ s 5 5

5- 25 DDR3-1600 Speed Bins and Operating Conditions

SpeedBin	DDR3-1600G (optional)	DDR3-1600H	DDR3-1600J	DDR3-1600K

5.3.8 DDR3

5- 26 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Timing										
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	8	-	ns
Average Clock Period	tCK(avg)									ps
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg) min + tJIT(per)min	tCK(avg) max + tJIT(per) max	tCK(avg) min + tJIT(per)min	tCK(avg) max + tJIT(per) max	tCK(avg)min + tJIT(per) min	tCK(avg) max + tJIT(per) max	tCK(avg)min +		

Cumulative error across 10 cycles	tERR(10per)	-257	257

Mode Register
Set command
update delay

Power-up and RESET calibration time	tZQinit	max(512nCK,640ns)	-	max(512nCK,640ns)	-	max(512nCK,640ns)	-	max(512nCK,640ns)	-	
Normal operation Full calibration time	tZQoper	max(256nCK,320ns)	-	max(256nCK,320ns)	-	max(256nCK,320ns)	-	max(256nCK,320ns)	-	
Normal operation Short calibration time	tZQCS	max(64nCK,80ns)	-	max(64nCK,80ns)	-	max(64nCK,80ns)	-	max(64nCK,80ns)	-	
Reset Timing										
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK,tRFC(min)+10ns)	-	max(5nCK,tRFC(min)+10ns)	-	max(5nCK,tRFC(min)+10ns)	-	max(5nCK,tRFC(min)+10ns)	-	
Self Refresh Timings										
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE(min) + 1 nCK	-	tCKE(min) + 1 nCK	-	tCKE(min) + 1 nCK	-	tCKE(min) + 1 nCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	
Power Down Timings										
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK,7.5ns)	-	max(3nCK,7.5ns)	-	max(3nCK,6ns)	-	max(3nCK,6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCK,24ns)	-	max(10nCK,24ns)	-	max(10nCK,24ns)	-	max(10nCK,24ns)	-	

CKE minimum pulse width	tCKE	max(3nCK 7.5ns)	-	max(3nCK ,5.625ns)	-	max(3n CK,5.62 5ns)	-	max(3n CK,5ns)	-	
Command pass disable delay	tCPDED	1	-	1	-	1	-	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(mi n)	9*tREFI	tCKE(mi n)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	1	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	1	-	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(t WR/tCK(a vg))	-	WL+4+(t WR/tCK(a vg))	-	WL+4+(tWR/tC K(avg))	-	WL+4+(tWR/tC K(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+W R+1	-	WL+4+W R+1	-	WL+4+ WR+1	-	WL+4+ WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL+2+(t WR/tCK(a vg))	-	WL+2+(t WR/tCK(a vg))	-	WL+2+(tWR/tC K(avg))	-	WL+2+(tWR/tC K(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL+2+W R+1	-	WL+2+W R+1	-	WL+2+ WR+1	-	WL+2+		

Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	2	8.5	ns
RTT turn-on	tAON	-400	400	-300	300	-250	250	-225	225	ps
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timings										
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	325	-	245	-	195	-	165	-	ps
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	325	-	245	-	195	-	165	-	ps
Write leveling output delay	tWLO	0	9	0	9	0	9	0	7.5	ns
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns

5.4 RGMII

RGMII VDD_3V3 3.3V

5.4.1 RGMII

5-27 RGMII

Ioh	(VDDE-0.4V)	12	mA
Iol	(0.4V)	12	mA

5- 30 USB

Parameter	Symbol	Conditions	Min.	Max.	Units
InputLevelsforLow-/full-speed:					
High(driven)	VIH		2		V
High(floating)	VIHZ		2.7	3.6	V
Low	VIL			0.8	V
Differential Input Sensitivity	VDI	|(D+)-(D-)|	0.2		V
Differential Common Mode Range	VCM	Includes VDI range	0.8	2.5	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal amplitude)	VHSSQ		100	150	mV
High speed disconnect detection threshold (differential signal amplitude)	VHSDSC		525	625	mV
High-speed differential input signaling levels					
High-speed data signaling common mode voltage range(guide line for receiver)	VHSCM		-50	500	mV
Output Levels for Low-/full-speed:					
Low	VOL		0	0.3	V
High(Driven)	VOH		2.8	3.6	V
SE1	VOSE1		0.8		V
Output Signal Crossover Voltage	VCRS		1.3	2	V
Output Levels for High-speed:					
High-speed idle level	VHSOI		-10	10	mV
High-speed data signaling high	VHSOH		360	440	mV
High-speed data signaling low	VHSOL		-10	10	mV
Chirp J level(differential voltage)	VCHIRPJ		700	1100	mV
Chirp K level(differential voltage)	VCHIRPK		-900	-500	mV
Decoupling Capacitance:					
Downstream Facing Port Bypass Capacitance (perhub)	CHPB	VBUS to GND	120		F
Upstream Facing Port Bypass Capacitance	CRPB	VBUS to GND	1	10	F
Input Capacitance for Low-/full-speed:					
Downstream Facing Port	CIND			150	pF
Upstream Facing Port(w/ocable)	CINUB			100	pF
Transceiver edge rate control capacitance	CEDGE			75	pF
InputImpedanceforHigh-speed:					
TDRspecforhigh-speedtermination					

Term_ e (Ƙ ˜ "Ą ´ Ƽ

5.6 Flash

6

6.1

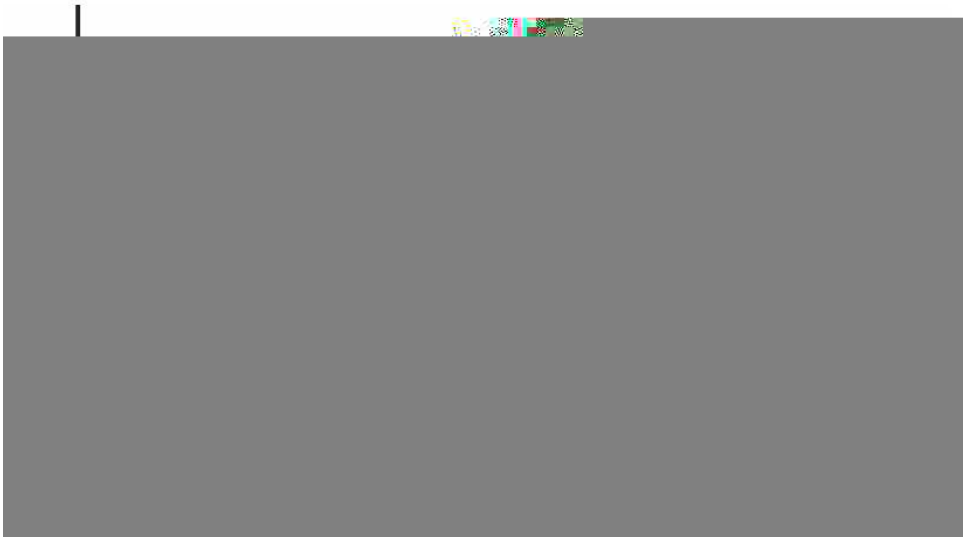
6- 1

Parameter	Value
TDP Max Power	5 Watts
Rth(J-C)	6 ÁC/W
Tj	125 ÁC

6.2

6- 2

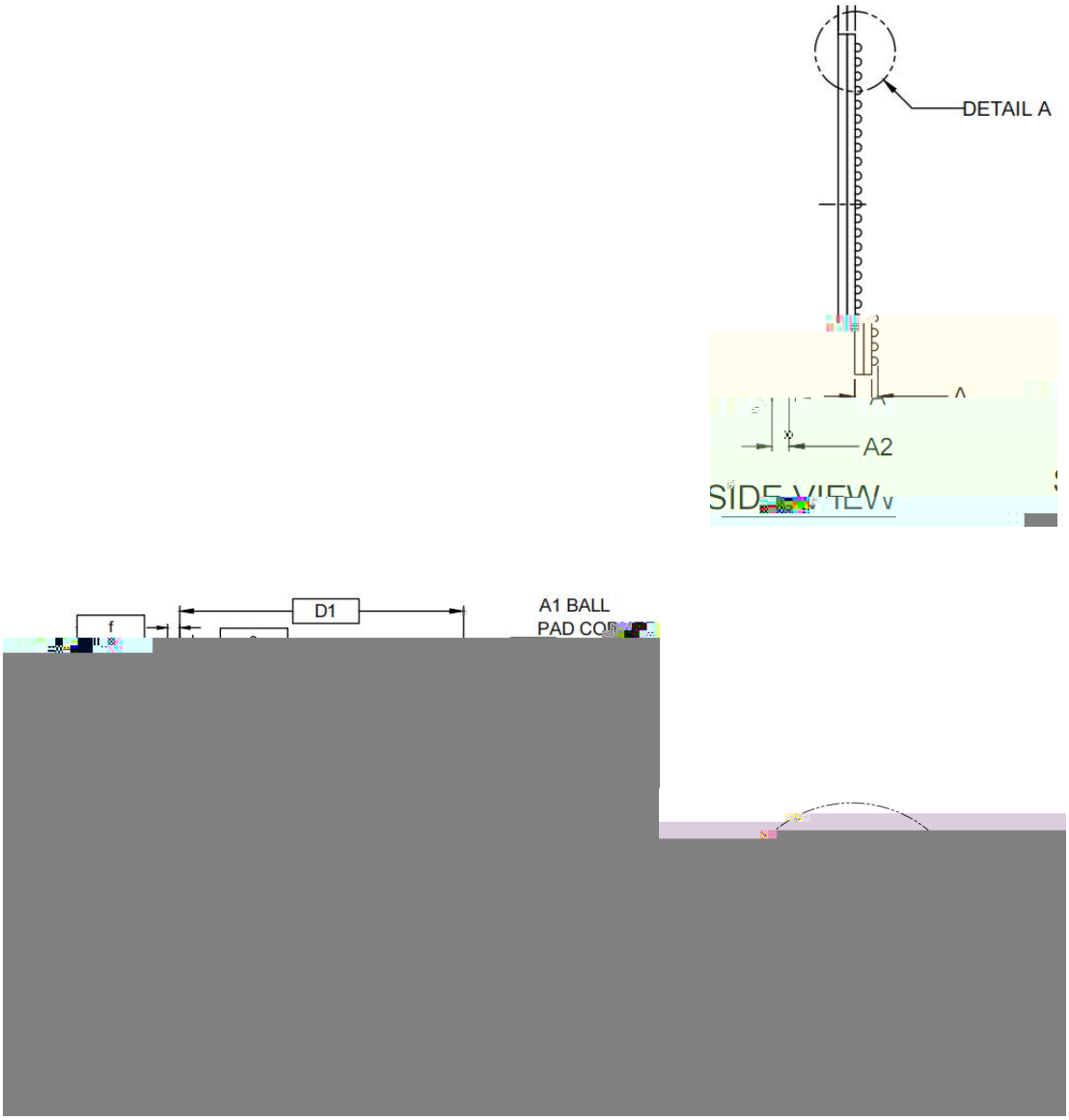
Profile Feature		Pb-Free Assembly
Average ramp-up rate (Tsmax to Tp)		3ÁC/second max.
Preheat	Temperature Min (Tsmin)	150 ÁC
	Temperature Max (Tsmax)	200 ÁC
	Time (Tsmin to Tsmax) (ts)	60-180 seconds
Time maintained above	Temperature (TL)	217 ÁC
	Time (tL)	60-150 seconds
Peak Temperature (Tp)		245ÁC
Time within 5ÁC of actual Peak Temperature (tp)2		20-40 seconds
Ramp-down Rate		6 ÁC/second max.
Time 25ÁC to Peak Temperature		8 minutes max.



6.1

	20	21	22	23
A	DDR_DQ16	DDR_DQSP2	VSS	VSS
B	DDR_DQM2	DDR_DQSN2	DDR_DQ19	VSS
C	DDR_WEN	DDR_DQ17	DDR_DQ21	DDR_DQ23
D	<DUMMY_NET>	DDR_DQ18	DDR_DQ20	DDR_DQ22
E	<DUMMY_NET>	VSS	DDR_DQ24	
F	<DUMMY_NET>	DDR_DQM3	DDR_DQ25	DDR_DQ26
G	<DUMMY_NET>	VSS	DDR_DQ27	

7.2



7.2

7- 2

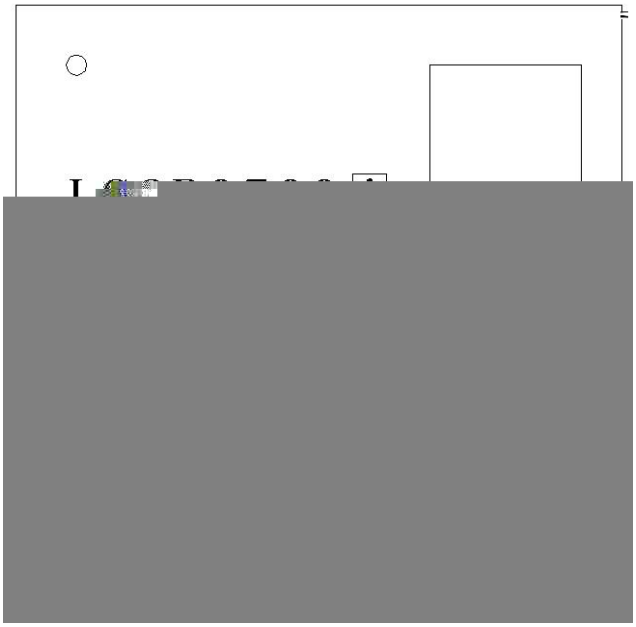
NOTE:

1. DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2009.
3. TERMINAL POSMONS DESIGNATION PER JESD 95.
4. REFLOW BALL DIAMETER.
5. DIMENSION ñbò IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
6. RAW SOLDER BALL SIZE DURING ASSEMBLY IS

8

8-1 –

9



9.1

a) ○

b) LS2P0500 LS2P0500 A -i

c) CHN YYWW VV H

d) VDAAAAAAANNNN

e) LOONGSON È

f) c
